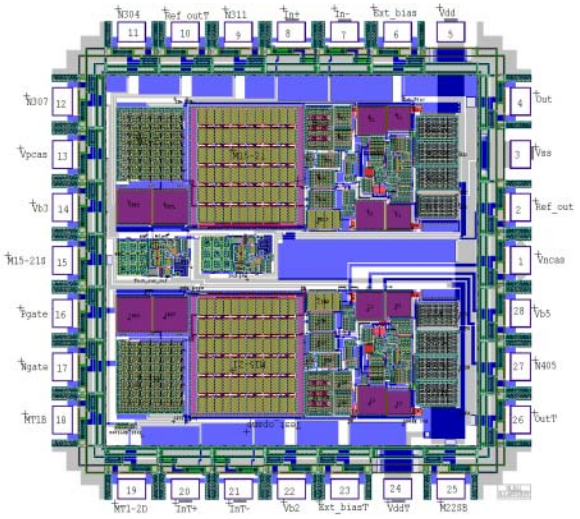
# Microelectronic Training Program Overview



**Objective**
To be able to do state-of-the-art analog design in digital CMOS processes, including BiCMOS.

**Description**
A formal program of self-education with course work in CMOS analog design and layout. The final project is a low-noise 10.6MHz CMOS opamp with 20mA output, now in fabrication at MOSIS. Layout shown **at right**. Schematic is **below**.

**Courses**

- M501 Basic BiCMOS Analog IC Design (completed)
- M511D MOSIS Project (completed)
- M601 HDL Design (completed)
- M512 MOSIS Project Evaluation and Report (scheduled)
- M502 Advanced CMOS IC Design (scheduled)
- M503 High Speed and RF CMOS Analog IC Design (scheduled)

**Duration**
The first phase, comprising M501, M502 and the M511D project ran from 9/28/06 to 2/21/09 (29-months). Most of that time was spent on the CMOS opamp design and layout. A substantial portion was devoted to evaluating, learning and working with multiple simulation and multiple layout tools. Education is continuing with the second phase, which includes M502, M503 and the M512 chip evaluation to come.

**Documents Available for Review**

- SL511 Design Review Package - Brief design review document for the CMOS opamp chip.
- M511D Design Notes - ~500-pages of typed and illustrated notes on the CMOS opamp design.
- M501 Syllabus
- M501 Term Paper - ~40-pages, "An Overview of BiCMOS Analog IC Design"
- M501 Homework
- M601 Syllabus
- M601 Project Report - Verilog programming an FPGA to produce a sawtooth output from a 16-bit serial DAC.
- M601 Homework
- Verilog FAQ - Answers to questions which weren't addressed in tutorials.